

WHAT IS CLAIMED IS:

1. An image processor comprising:
- image memory which stores image data;
- an image memory control unit which is connected to an
- 5 image reading unit for reading image data, and/or an image processing unit for processing and editing image data, and/or an image writing unit for writing image data to transfer paper or the like; receives first image data read-in by said image reading unit and/or second image data subjected to image
- 10 processing by said image processing unit; transmits the first image data and/or the second image data to said image memory; and transmits the image data stored in said image memory to said image processing unit and/or said image writing unit;
- a system control unit which controls transmission or
- 15 reception of control signals used in each of said units or between said units; and
- a source detection unit which detects a source of image data to said image memory control unit; wherein
- said system control unit controls said image memory
- 20 control unit according to the source of the image data detected by said source detection unit, and determines a transmission order of the image data to said image memory.

determines that the image data is larger than said predetermined volume.

6. The image processor according to claim 1 further comprising:

an image data expansion unit which expands the image data; and

a compression determination unit which determines whether the image data has been compressed, wherein

10 said image memory control unit provides controls so as to transmit the image data to said image data expansion unit when said compression determination unit determines that the image data has been compressed.

15 7. An image processor comprising:

an image reading unit which acquires an image data;

an image processing unit which processes the image data acquired by said image reading unit;

20 an image memory which stores the image data acquired by said image reading unit or the image data processed by said image processing unit;

an image memory control unit which receives data sent from said image reading unit or image processing unit, and receives the data sent from said image memory and transmits
25 it to said image reading unit or image processing unit;

a system control unit which controls transmission or reception of data by said image memory control unit; and

a detection unit which detects which one of said image reading unit or image processing unit has transmitted the image data to said image memory control unit,

wherein said system control unit controls said image memory control unit based on the detected source of the image, and determines the order in which the image data is to be transmitted to said image memory.

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8. An image processor comprising:

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image memory for storing image data;
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an image memory control means which is connected to
an image reading means for reading image data, and/or an image
15 processing means for processing and editing image data, and/or
an image writing means for writing image data to transfer
paper or the like; receives first image data read-in by said
image reading means and/or second image data subjected to
image processing by said image processing means; transmits
20 the first image data and/or the second image data to said
image memory; and transmits the image data stored in said
image memory to said image processing means and/or said image
writing means;

a system control means for controlling transmission
25 or reception of control signals used in each of said units

or between said means; and

a source detection means for detecting a source of image data to said image memory control means; wherein

said system control means controls said image memory control means according to the source of the image data detected by said source detection means, and determines a transmission order of the image data to said image memory.

9. The image processor according to claim 8, wherein said image memory control means is connected to said one or more means through an image data control means,

wherein said image data control means performs transmission or reception of image data between said image memory control means and said one or more means.

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10. The image processor according to claim 8, wherein said image memory, said image memory control means, and said system control means are formed as a discrete controller means.

11. The image processor according to claim 8, wherein said image memory control means has a bus control means for controlling a bus connected to said one or more means.

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14. An image processor comprising:
an image reading means for acquiring an image data;
an image processing means for processing the image data
acquired by said image reading means;
5 an image memory for storing the image data acquired
by said image reading means or the image data processed by
said image processing means;
an image memory control means for receiving data sent
from said image reading means or image processing means, and
10 receives the data sent from said image memory and transmits
it to said image reading means or image processing means;
a system control means for controlling transmission
or reception of data by said image memory control means; and
a detection means for detecting which one of said image
15 reading means or image processing means has transmitted
the image data to said image memory control means,
wherein said system control means controls said image
memory control means based on the detected source of the image,
and determines the order in which the image data is to be
20 transmitted to said image memory.